Abstract-- A 0.35 µm op-amp configuration with a slew rate in excess of 10 V/µs and a unity gain bandwidth of 5 MHz with load capacitance of 10 pf is proposed. Dynamic technique that runs on a large current source when the rate of change of input is larger than a pre-decided value. All the operational amplifier parameter like Common Mode Rejection Ratio (CMRR), Input Common Mode Ratio (ICMR), Open loop gain, Bandwidth, unity gain bandwidth, are same before and after the Dynamic bias circuit is added.

Keywords – Common Mode Rejection Ratio, Complementary metal Oxide Semiconductor, Input Common Mode Ratio, Open Loop Gain, Output Offset Voltage, Width/Length.

I. INTRODUCTION

This paper relates to operational amplifiers and more particularly to a high precision operational amplifier which is intermittently operational and providing a low quiescent power requirement when in stand by state while proving high slew rate when activated.

CMOS Op-amps typically have their slew rates of the order of 10 V/ns. CMOS opamps with their slew rates an order of magnitude larger have been proposed. Dynamic current boosting is a popular technique employed to increase the slew rate. In [1], a large current source is turned on whenever the input crosses a preset value of slope.

\[ \text{Slew Rate} = \frac{I}{C} \]  

Thus, for a given capacitance, the power consumption imposes a definite limit to the slew rate. A possible solution controlled input stage or dynamic biasing [1].

For stand by operation, circuits are turned off very briefly and then powered down as quickly as possible to minimize power consumption.

II. DESIGN

As shown in fig-1 is the block diagram of high slew rate operational amplifier. We require high slew rate as well as low power consumption. Slew Rate depends upon two parameter current and load capacitance but we can not play with load capacitance. Only design parameter is current but if we increase current statically then power dissipation will increases.

By taking this specification started the design of the op-amp [4] and calculating the (W/L) ratio of fig-2. First assume that \( V_{SG4} = V_{SG6} \). This will cause “proper mirroring” in the M3-M4.
mirror. Also, the gate and drain of $M_4$ are at the same potential so that $M_4$ is "guaranteed" to be in saturation. So if the balance condition is satisfied, then $V_{DG4} = 0$ and $M_4$ is saturated.

B. Proposed Dynamic Bias Circuit

As shown in fig-1 both input are connected in dynamic bias circuit. Consider $V_{in+}$ input we first require differentiator so when out input speed is high then our circuit become active. Here, we take square wave input for checking purpose. So our differentiator output spike is coming. Spike output is depending on differentiator circuit. RC circuit is used as differentiator. Output is depending upon three parameter $R$, $C$ and input speed (rise time and fall time). So these three are our design parameter. We design the circuit like that if our input speed is decrease than 10ns than spike output value is near about 1v. So this 1v output can turn-on other MOS circuit. $M_9$ and $M_{10}$ are act as differentiator for $V_{in+}$. $M_9$ acts as MOS capacitor. And $M_{10}$ act as MOS Resistor. PMOS is used as resistor because of mobility of hole is less than electron. So PMOS gives high resistance value.

Now consider 1v positive and 1v negative spike comes at the input of $M_{11}$ and $M_{12}$. During positive spike $M_{11}$ turns on and during negative spike $M_{12}$ turns on. So current is flowing through that during short amount time. Here $M_{13}$ and $M_{14}$ transistor are in fixed bias. So current flowing through it is constant. Whenever high current flow then drain node voltage is increase because of loading effect. So it can turn on the transistor $M_{15}$ and $M_{16}$ which is heavy current sink so near about 1mv dynamic current is flowing in the circuit during transition so our slew rate increase. Total three main parts of dynamic circuit differentiator, Comparator, Heavy Current sink. As shown in fig-3 transistor $M_9$ and $M_{10}$ are work as differentiator for $V_{in+}$, $M_{11}$, $M_{12}$, $M_{13}$, $M_{14}$ are work as comparator for both and $M_{15}$ and $M_{16}$ work as heavy current sink. For $V_{in-}$ $M_{18}$, $M_{17}$ work as differentiator and rest part are same.

By considering the load capacitance 10pf we proposed our design and calculating the (W/L) of the figure 3.

III. SIMULATION RESULTS

Simulation is more concentration on Slew rate. Slew rate is nothing but how fast output can swing without distorted. For this we are apply pulse (i.e. $V_{in+}$ 2 0 PULSE (-1v 1v 0ns 2ns 2ns 10µs 50µs)) and checking the output with and without the dynamic bias circuits as shown in fig-5 and fig-4 respectively in SPICE. Now we have to also consider other parameter of op-amp that is not to be change by after applying the dynamic bias circuit.

I) For open loop gain calculation we apply a sinusoidal signal ($V_{in+}$ 2 0 SIN (0 100u 1k)) at the input of op-amp with 10pf load capacitor.

II) For ICMR we apply DC input ($DC V_{in+}$ -2.5v 2.5v 0.1v) at the input terminal with stepping of 0.1v

III) For output offset voltage we apply small amount of voltage ($DC V_{in+}$ -5mv 5mv 1mv) at input with stepping of 1mv.

IV) For CMRR we apply a common input to both terminal and calculate using $CMRR=20\log(Ad/Ac)$.

<table>
<thead>
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<th>TABLE III</th>
<th>OP-AMP PARAMETERS WITH AND WITHOUT BIAS CIRCUIT</th>
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<tr>
<td>Technology</td>
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<tr>
<td>Open loop gain</td>
<td>9984 v/v</td>
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<tr>
<td>$V_{dd}$</td>
<td>2.5 V</td>
</tr>
<tr>
<td>$V_{ss}$</td>
<td>-2.5 V</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>9.09 v/µs</td>
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<tr>
<td>ICMR</td>
<td>-1 to 2v</td>
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<td>Unity Gain Bandwidth</td>
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<td>Phase margin</td>
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<td>CMRR</td>
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</tbody>
</table>

![Fig-2 Operational Amplifier](image)

![Fig-3 Dynamic Bias Circuit](image)
V. CONCLUSIONS

Slew rate of operational amplifier is depending on two parameter capacitance and current flowing through circuit. Capacitor is not design parameter so the only one design parameter is current but if increase current statically the power dissipation in the circuit is increases. So, concept of dynamic biasing is come to picture. So design the operational amplifier with dynamic biasing circuit we can achieve less power dissipation and high slew rate at the same time.

REFERENCES