PV SYSTEM BASED FPGA: ANALYSIS OF POWER CONSUMPTION IN XILINX XPOWER TOOL

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Abstract – In this paper we study a methodology to integrate a PV power source with energy storage battery backup device and generate power by an innovative Solar Power inverter. The use of software based Direct PWM modulation strategy and its soft control feature extend the flexibility to control inverter parameters like voltage, frequency number of PWM pulses etc without changing any hardware circuit. The system simulation of PWM Pulse generation has been done on a XILINX based Spartan 3E board using Verilog code. The test on simulation of PWM generation program after synthesis and compilation were recorded and verified on a prototype circuit. Field-programmable gate arrays (FPGAs) are pervasive in embedded systems requiring low-power utilization. [1] A novel power optimization methodology for reducing the dynamic power consumed by the routing of FPGA circuits by modifying the constraints applied to existing commercial tool sets is presented. The power optimization techniques influence commercial FPGA Place and Route (PAR) tools by translating power goals into standard throughput and placement based constraints. [5]

Keywords: FPGA: Field Programmable Gate Array, PWM: Pulse Width Modulation, PV: Photovoltaic,

I. INTRODUCTION

The Pulse width modulated (PWM) adaptive intelligent Power converter (inverter) has been designed and developed where the input DC power stored in the battery bank obtained through PV and/or Grid sources, has been digitized to produce a sequence of PWM pulses (approximate to a sine wave) at the output of power converter and deliver power to the load. The traditional analog method for generating PWM pulses adopt the technology where a high frequency carrier signal is compared with sinusoidal wave as reference signal set at desired output frequency and thus needed two signals to produce PWM signal. [1] In the present scheme, the PWM pulses are directly generated through software programme using Verilog codes and downloaded in FPGA Spartan 3E starter kit to produce base drive signals for inverter power device switches. [2] The FPGA technology offers a fast system with many more advantages as compared to other conventional technology including DSP based controller. The software programme can easily be changed to optimize and control the inverter parameters like frequency, voltage amplitude, number of half cycle PWM pulses etc. without changing the hardware circuit.

II. SYSTEM CONFIGURATION

![Fig.1 Block diagram of Solar Power Inverter](image-url)
The system works under two modes of its operation namely:

- Charging Mode (Grid available Period)
- Inverting Mode (Grid Cut off or restricted Period)

III. PV SYSTEM

The Grid-connected PV system is divided into two categories according to function: one is non-scheduling type without battery; another is schedulable type with battery. The system block diagram is shown in Figure 1. The schedulable Grid-connected PV system has significant expansion and improvement than the non-scheduling system in the way of function and performance. First, the core controller generally consists of two main parts- Grid inverter and battery charger. Its function is not only to be able to inverter DC after the transmission to the grid, but also to charge the battery. Second, the system is equipped with the main switch and an important load switches.

When the AC power grid power is interrupted the core controller disconnect the grid main switch, but the important load switch remains closed so as to the DC power provided by solar arrays and batteries still supply important AC loads.

Generally, in PV system the control core is made up of DSP or SCM whose disadvantage is that the whole system has more separate components and bad stability. In this paper, an alternative system architecture based on FPGA is provided to replace the above-mentioned. FPGA has many advantages such as large-capacity, high speed, low power consumption and so on, and the SCM or DSP controller core can be embedded in FPGA. So FPGA can greatly improve system integration, enhance system reliability, and reduce system cost.

IV. PV SYSTEM GENERAL SCHEME BASED FPGA

The grid PV system is schedulable type, and its control core is FPGA which complete all control and operation work. FPGA unit consists of several modules: MCU, PWM and data process, etc. MCU module is responsible for coordination throughout the system control, such as Human-Computer Interaction Information Processing, to control battery charging and discharging, to control PWM and to process other emergencies; PWM module's function is under the control of the MCU to generate PWM signal, which is delivered to convertor to convert the DC from storage battery to AC, which can directly drive AC loads or be added to the power network after phase synchronization; Data process module is used to compute the parameter’s value, which contains direct voltage, direct current, direct current power, storage battery charging and discharging state, power network phase, MPPT(maximum power point tracking), monitoring, the system's total generated energy, etc.

This system adopts the current control method based on PWM, which can be gained through processing the sampling signal and can be used to drive the former MOSFET / IGBT. The System's overall work process is relatively simple. The first is system initialization, which contains PWM initialization, capture initialization and A/D initialization. And then the timer is started to enter the loop waiting for interrupts. [4]

A. Inverter function strategy

There are many ways to achieve inverter function in PV system, in which full-bridge method based on PWM is usually adopted. The important link in this scheme is pulser and genlock, so the control system is relatively complex. There is also a relatively new control strategy that the power network voltage signal is using the given signal to trace current, and the sinusoidal output current in phase with the power network voltage can be gained.

B. AC parameters sample strategy

The way of sampling AC parameters generally contains synchronous sampling, quasi-synchronous sampling, non-synchronous sampling, non-integer-period sampling, etc. Among them, synchronous sampling is also called interval the whole cycle of sampling, which contains hardware synchronous sampling and software synchronous and is a more common method to measure AC parameters.

In this system software synchronous sample scheme is implemented through the MCU module which is the part of FPGA. MCU measures the power network cycle through capturing level
changing and calculates the sampling time interval, and then gives the synchronous pulse to start sampling.

C. Grid-connected current control strategy

Controller's output current and the power grid must be in phase with the same frequency in order to achieve generation system's power be added to the power network safely. So this system adopts a control strategy which combines dual-loop phase-locked and synchronization. Inner loop phase control system is used to real-time track current. Outer loop phase control system is used to eliminate the error generated by inner control. Synchronous phase-locked loop is used to generate synchronized pulse with the grid voltage reference current signal.

There have been many FPGA power reduction approaches addressing different design levels. Several techniques for low power FPGA design have appeared in literature addressing the VLSI design of an FPGA.[10] Research has also considered various synthesis-level power optimizations, such as technology mapping to LUT-based FPGAs techniques or reducing glitching power through pipelining.

In today’s FPGAs about 50%-70% of total power is dissipated in the inter-connection network.

The dynamic power of nets is characterized by

\[ P_{\text{dynamic}} = \sum C_i * F_i * V^2 \]  

(1)

Where \( C_i \) and \( F_i \) are the capacitance and average toggle rate of the ith net, and \( V \) is the internal voltage. For a given net, the dynamic power can be reduced by diminishing its capacitance, or length. Nets with high toggle rates and/or high capacitance therefore are good potential targets for decreasing the overall power and serve as the motivation of the power optimization schemes presented.
VI. SOFTWARE BLOCK DIAGRAM

![Fig.4 Software Block Diagram of Intelligent controller]

In Software Design We give one Clk as input and three output PWM, SEL, WAVE1 and download it into Spartan 3E FPGA Kit and analysis their output.

![Fig.5 Xilinx Spartan 3E FPGA Kit]

VII. SOFTWARE XPOWER ANALYSIS RESULTS USING PLACE AND ROUTE METHODS FOR POWER CONSUMPTION OF PROGRAM

As a solar system designer, we should choose our solar inverter based on low energy consumption and high efficiency. The efficiency indicates the percentage of the available solar power that is actually converted and fed into the utility grid. Modern inverters currently consume between 4 and 8 % of the converted energy in the conversion process, which corresponds to an overall efficiency of 92 to 96%.

Further reducing this already low energy consumption is a major technical challenge, and one which can only be achieved with new and innovative designs.

In these tables we show that our software consumes low energy means low Power design based on VLSI FPGA technique and these Power data are analyze through XPOWER tool of Xilinx Software and results are shown in table. [12]

A. Generate Power Data

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vccint</td>
<td>1.2</td>
<td>0-100</td>
</tr>
<tr>
<td>Vcco25</td>
<td>2.5</td>
<td>-</td>
</tr>
<tr>
<td>Total Power</td>
<td>-</td>
<td>- 120</td>
</tr>
</tbody>
</table>

B. Power Data

<table>
<thead>
<tr>
<th>Power Summary</th>
<th>Typical P (mW)</th>
<th>Worst Case P (mW)</th>
<th>% diff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Estimated Power Consumption</td>
<td>120</td>
<td>120</td>
<td>0</td>
</tr>
<tr>
<td>Vccint 1.2 (V)</td>
<td>120</td>
<td>120</td>
<td>0</td>
</tr>
<tr>
<td>Vcco25 2.5 (V)</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>Logic</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>Vcco25</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>Signals</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>Quiescent Vccint 1.2 (V)</td>
<td>120</td>
<td>120</td>
<td>0</td>
</tr>
</tbody>
</table>

VIII. CONCLUSION & FUTURE WORK

This paper presents a PV grid-connected control system scheme based on FPGA, which expanded the scheme to build solar power generation system and can effectively control the battery charging and discharging and the power to be added to network. In addition, due to the FPGA as the core building control system it makes the system more compact and simple structure, which improves the stability, while reducing power consumption.
The use of FPGA technology to generate PWM pulses for solar inverter using Verilog programming language has successfully been implemented in the present study. The software controlled programme can alter the inverter parameter(s) and can easily be outputted through FPGA board.

IX. REFERENCES

[1] FPGA-Based PWM Intelligent Adaptive Solar Inverter as a Utility Interface for Use in Agro-Based Application by Dr. S.N.Singh and Dr. A.K.Singh
[2] A Novel Design of Sustainable Solar Home Power Lighting: A Case Study with Indian Restaurant by Dr. S.N.Singh and NishaKumari
[4] The Study in Photovoltaic Control System Based on FPGA by Jiuhua Zhang, Fengde Guo