3EC04: CMOS DIGITAL INTEGRATED CIRCUITS
CREDITS – 3 (LTP: 3,0,0)

Course Objective:

The course intends to provide an understanding of the building blocks for microprocessor/microcontroller or digital VLSI circuit based on the MOS circuit. The main focus in this course is on the transistor circuit level design and realization for digital operation and the issues involved in CMOS design.

Teaching and Assessment Scheme :

Teaching Scheme (Hours per Week)			Credits	Assessment Scheme				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE	CE	ESE	CE	
3	0	0	3	60	40	00	00	100

Course Content :

Unit No.	Topics	Teaching Hours
1.	**Introduction and Fabrication of MOSFET :** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, Style for digital system design, Design quality, package technology, introduction to FPGA and CPLD, computer aided design technology. Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	08
2.	**MOS Transistor & FinFET :** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current Voltage characteristics, MOSFET scaling and small geometry effects, MOSFET capacitances, FinFET: model(BSIM-CMG), physics and operation.	08
3.	**MOS Inverters: Static characteristics :** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load Enhancement and Depletion type MOSFET load, CMOS Inverter	06
4.	**MOS Inverters: Switching characteristics and Interconnect Effects :** Delay-time definitions, Calculation of Delay times, CMOS Ring oscillator Circuit, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters.	08
5.	**Combinational-Sequential and Dynamic MOS Logic Circuits :** Introduction, MOS logic circuits with Depletion NMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs). Behavior of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop. Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-	09

Unit No.	Topics	Teaching Hours
	performance Dynamic CMOS circuits.	
6.	**Chip I/P, O/P Circuits, Design for testability and Introduction to FINFET :** On chip Clock Generation and Distribution, Latch –Up and its Prevention. Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self-Test (BIST) techniques, current monitoring IDDQ test.	06
	Total	**45**

List of References :

1. Sung – Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated circuits – Analysis and Design*", 3 edition, Mc Graw Hill Education, 2002
2. Adel S. Sedra, Kenneth C. Smith, "*Microelectronic Circuits*", Sixth Edition, Oxford University, 2013.
3. Douglas A. Pucknell and Kamran Eshraghian, "*Basic VLSI Design*", 3rd edition, PHI Learning, 2009.
4. John P. Uyemura , "*Introduction to VLSI Circuits & Systems*" 1st edition, Wiley, 2001
5. Yogesh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal Juan Duarte ,Navid Payvadosi, Ai Niknejad, Chenming Hu "*FinFET Modeling for IC Simulation and Design*", 1st edition, BSIM-CMG Standard , 2015.

Course Outcomes (COs):

1. Understand the fabrication process of IC technology and VLSI design flow.
2. Analyze the electrical and physical properties of MOSFET.
3. Have an understanding of the static and switching characteristics of MOSFET based circuit.
4. Analyze, understand the design of Combinational, Sequential and dynamic Logic circuits.
5. Develop the understanding of CMOS latch-up, clocking strategy, and testing principles.
6. Develop the CMOS based digital circuits to solve the real-life problem.